

a sidewall section formed upright around said mounting portion of said first insulating substrate;

a cavity defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion; and

a second insulating substrate provided in said cavity and on said sidewall section and carrying a second electrically conductive pattern electrically connected to said first electrically conductive pattern via through-holes formed in said sidewall section;

wherein solder lands are provided at least in said cavity on one surface of said first insulating substrate,

wherein a heat radiating plate is provided on an opposite surface of said first insulating substrate.

4. (amended) A semiconductor package comprising:

a first insulating substrate carrying a mounting portion for mounting a semiconductor device and a first electrically conductive pattern electrically connected to said semiconductor device;

a sidewall section formed upright around said mounting portion of said first insulating substrate;

a cavity defined by said first insulating substrate and the sidewall section and encapsulated by encapsulating resin as said semiconductor device is mounted on said mounting portion; and

a second insulating substrate provided in said cavity and on said sidewall section and carrying a second electrically conductive pattern electrically connected to said first electrically conductive pattern via through-holes formed in said sidewall section;

wherein solder lands are provided at least in said cavity on one surface of said first insulating substrate,

wherein said second insulating substrate is a laminated sheet lined on one side with copper.

7. (amended) A method for the preparation of a semiconductor package comprising the steps of:

forming a mounting portion for mounting a semiconductor device and a first electrically conductive pattern for electrically connecting the semiconductor device on a first insulating substrate;

layering a spacer having an opening of substantially the same size as said mounting portion in one surface of said first insulating substrate;

mounting a semiconductor device in said mounting portion defined by said first insulating substrate and the opening provided in said spacer;

encapsulating said cavity with encapsulating resin after mounting said semiconductor device in said mounting portion;

layering a second insulating substrate carrying the a second electrically conductive pattern on one surface thereof on said spacer;

forming a through-hole for establishing electrical connection between said first electrically conductive pattern and said second electrically conductive pattern; and

forming solder lands at least on said cavity on said electrically conductive pattern,

wherein said second insulating substrate is a laminated sheet lined on one side with copper.

8. (amended) A method for the preparation of a semiconductor package comprising the steps of:

forming a mounting portion for mounting a semiconductor device and a first electrically conductive pattern for electrically connecting the semiconductor device on a first insulating substrate;

layering a spacer having an opening of substantially the same size as said mounting portion in one surface of said first insulating substrate;

mounting a semiconductor device in said mounting portion defined by said first insulating substrate and the opening provided in said spacer;

encapsulating said cavity with encapsulating resin after mounting said semiconductor device in said mounting portion;

layering a second insulating substrate carrying the a second electrically conductive pattern on one surface thereof on said spacer;

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forming a through-hole for establishing electrical connection between said first electrically conductive pattern and said second electrically conductive pattern;

forming solder lands at least on said cavity on said electrically conductive pattern; and

providing a heat radiating plate on the opposite surface of said first insulating substrate after forming said second electrically conductive pattern.

Please add the following new claims.

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9. (new) The semiconductor package according to claim 2, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

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10. (new) The semiconductor package according to claim 2, wherein said encapsulating resin is planarized.

11. (new) The semiconductor package according to claim 2, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

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some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

12. (new) The semiconductor package according to claim 4, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

13. (new) The semiconductor package according to claim 4, wherein said encapsulating resin is planarized.

14. (new) The semiconductor package according to claim 4, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

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some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

15. (new) The method according to claim 7, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

16. (new) The method according to claim 7, wherein said encapsulating resin is planarized prior to said step of layering said second insulating substrate.

17. (new) The method according to claim 7, wherein said second insulating substrate includes a cavity surface and a connection surface,

said cavity surface being adjacent and in contact with said cavity and said sidewall section, said connection surface being opposite said cavity surface,

said connection surface having a plurality of external electrical connections thereon, an external electrical connection of said plurality of external electrical connections providing a connection to an apparatus external from said semiconductor package,

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some external electrical connections of said plurality of external electrical connections being opposite said cavity, and other external electrical connections of said plurality of external electrical connections being opposite said sidewall section.

18. (new) The method according to claim 8, wherein said first insulating substrate is a laminated sheet lined on both sides of the insulating substrate with copper.

19. (new) The method according to claim 8, wherein said encapsulating resin is planarized prior to said step of layering said second insulating substrate.

20. (new) The method according to claim 8, wherein said second insulating substrate includes a cavity surface and a connection surface,